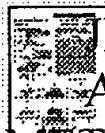


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**Patent Plaques**Recognize  
the achievement**JP11330295A2: INTEGRATED CIRCUIT  
ASSEMBLY AND ITS FORMING  
METHOD**[View Images \(1 pages\)](#) [View INPADOC only](#)Country: **JP Japan**Kind: **A2 Document Laid Open to Public Inspection**Inventor(s): **CHARLES W C LIN**Applicant(s): **ELLISTON INVESTMENT PTE LTD**  
[News, Profiles, Stocks and More about this company](#)Issued/Filed Dates: **Nov. 30, 1999 / Oct. 28, 1998**Application Number: **JP1998000307203**IPC Class: **H01L 23//12;**Priority Number(s): **May 2, 1998 SG1998000000994**

**Abstract:** **Problem to be solved:** To provide an assembly with a small section and high performance by directly metallizing a via hole and a bond pad for interconnecting an integrated circuit to a substrate circuit.

**Solution:** A via hole 306 on a dielectric substrate 304 is aligned to the upper part of a pad 302 of an integrated circuit chip 301 for entirely or partially exposing the pad 301 according to a side where a substrate faces. Then, an assembly is formed. After that, an electric conductive material is accumulated on the via hole 306 in addition to the surface of the I/O pad 301 of an integrated circuit to electrically and mechanically connect the chip 301 to a trace 305 of a dielectric circuit. In a connection method, the side wall of the via hole and the metal surface of a terminal pad are extended by electroless plating, are brought into contact each other, and are finally joined for forming an integration part, thus interconnecting terminal pads with extremely fine pitch.

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**Family**

<u>Patent</u>	<u>Issued</u>	<u>Filed</u>	<u>Title</u>
<a href="#">WO9957762A1</a>	Nov. 11, 1999	April 30, 1999	FLIP CHIP ASSEMBLY WITH VIA INTERCONNECTION
<b>JP11330295A2</b>	Nov. 30, 1999	Oct. 28, 1998	INTEGRATED CIRCUIT ASSEMBLY AND ITS FORMING METHOD
EP9957762W1	Nov. 11, 1999		
CN9957762W1	Nov. 11, 1999		
4 family members shown above			